Voltage Clamping for a Utility-Scale PV Array

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Abstract—Layout of the conductor material in the dc bus of a photovoltaic (PV) array to lower first cost and ohmic losses is reviewed. Six PV materials are characterized for their voltage swings from maximum power point to open circuit. A voltage-clamping shunt switch is proposed and experimentally verified to reduce the range of operating voltage in a utility-scale PV array, further improving its operating economy by reducing installed cost and ohmic losses.

Index Terms—Photovoltaic systems, fault voltage limiters, energy efficiency

I. INTRODUCTION

Solar PV will be an important component of future distributed generation (DG) systems due to its improving economics and green energy characteristics. Ongoing improvements in the cost and performance of the panels themselves must be matched by improvements in first cost and energy collection efficiency of the balance of system. This paper is motivated by a study of methods to improve the cost and efficiency of the inverter(s) and dc bus work in a utility-scale (>100 kW) PV system [7].

The key issue addressed in this paper is control of the array voltage level with regard to the ratings of the inverter and other components of the dc bus. All of the currently important PV panels require maximum-power-point tracking (MPP); that is, their dc voltage must be adjusted to an optimum level (V_{MPP}) to maximize energy production. The balance of system must be designed for efficient and economical performance at V_{MPP}. However, in the infrequent but unavoidable case where the ac grid has failed, or inverters have been shut down for maintenance, the entire system must safely withstand the worst-case panel open-circuit voltage (V_{OC}), typically much higher than V_{MPP}.

Rating the inverter switching devices for V_{OC} rather than V_{MPP} impacts their losses and costs. The higher voltage requirement also produces higher costs in dc fuses and switches as well. A voltage clamping system capable of reliably constraining the dc bus voltage such that it never exceeds V_{MPP} by any large amount is proposed.

This paper is organized as follows: First, various dc bus arrangements are reviewed, followed by the V_{OC}/V_{MPP} characteristics of six PV materials. Two configurations of a shunt voltage-clamping system are proposed. Finally, a sample implementation is designed and experimentally verified.

II. DC BUS ARRANGEMENTS

A. Centralized vs. Distributed Architectures

At the utility-scale, the prevailing dc bus configuration is series-connected strings of PV panels in sufficient numbers to reach the nominal voltage level of the array. These strings are then paralleled at combiner boxes, with the buses serving these further paralleled to achieve the capacity of the complete array. An “array” is here defined as the group of panels connected together for the purpose of MPP tracking. Each array may be serviced by one or multiple inverters having coordinated controls. Invariably an ac transformer is associated with each inverter, at which point the voltage level is increased enough to minimize copper costs and concerns with voltage drop. On the dc side of the inverter there is a tradeoff of first cost of the copper wire against energy collection efficiency.

Alternative configurations have been proposed [1]-[3], with more numerous (but smaller) inverters applied at the individual string level, or even at the individual panel level. The advantage of this approach is that MPP tracking is applied to smaller arrays, and voltage increase at the inverters will reduce wiring costs and losses. The concerns are bringing the first costs of these distributed power processors down to that of the central approach, and maintenance problems in finding faulty inverters. Clearly this approach would also mandate string- or panel-level monitoring.

A similar proposal uses distributed dc/dc converters to accomplish MPP tracking while producing a significant voltage increase. The total energy from a large collection of these arrays would then be processed by a central inverter.

B. Array Voltage Level

There are proponents for both the large array/central inverter and the small array/distributed inverter approaches. Nonetheless, this work assumes that at the utility scale, a relatively large array size will be selected, one composed of large numbers of panels distributed over a large area in both the x and y dimensions. It has previously been shown [4] that for a given energy loss or voltage profile, the total copper volume required is proportional to the square of the operating current. There is therefore good reason to design the system voltage as close as possible to the limits set by the panel manufacturers or any applicable safety standards, thus minimizing the required current.
Stated another way, the design voltage chosen will have increasing impact on the array energy harvest and copper costs as the size of the array is increased. Ultimately, the economic size of an array (defined as one MPP tracking unit) is limited by either the first cost of the copper required, or the statistics of possible differential shading.

C. Array Voltage Profile and DC Energy Losses

The same work [4] analyzed three alternative dc bus copper assignments. The constant area (CA) approach keeps the bus cross section constant over its length, with resulting variable current density and a parabolic voltage drop distribution over distance. The proportional area (PA) approach keeps the current density constant over its length and produces a linear voltage drop over distance. The constant-voltage-drop (CVD) approach uses a segmented bus construction that results in the same voltage drop at every point along the distance of the bus. For a given system voltage and volume of copper to use in the bus, the PA approach gives the lowest energy loss in the bus, while the CVD approach yields the same operating voltage at every panel in a large array (assuming that all panels are identical). The CVD approach reduces MPP mismatch problems throughout a large array. All three techniques are approximated by various current installation practices.

Another useful conclusion [4] is that the inverter should be physically located at the center of the bus that feeds it. If it is moved to an end of the bus, the energy losses will increase by 4 times, or else 4 times the volume of copper must be used in the bus to restore the previous level of loss. This is equally true for all three bus arrangements considered.

Some novel array wiring practices have been proposed [5]-[6], but are not yet used in practice to the authors’ knowledge. The “total cross tied” (TCT) and “bridge linked” (BL) configurations use series strings paralleled at collection buses, but with some additional wiring connections. The BL approach adds a systematic pattern of jumpers interconnecting key points of every two adjacent strings. The TCT approach carries this further with an extensive interconnection of every corresponding internal node of every string in the array. The intent of both of these techniques is mitigation of the panel mismatch effects on MPP tracking. Simulation studies suggest significant improvement of array energy harvesting. However, the installation appears complicated, and the fault protection of the strings would be daunting.

III. PV PANEL CHARACTERISTICS

Six PV panel materials were considered as representative of currently used technologies. These are 1) crystalline silicon (c-Si), 2) polycrystalline silicon (poly-Si), 3) amorphous silicon (a-Si), 4) gallium arsenide (GaAs), 5) cadmium telluride (CdTe), and 6) copper-indium-diselenide (CIS). The design issues involved in using these solar panels are illustrated by considering two operating points: The first is VMPP at full power operation; the second is VOC under the worst-case conditions likely in the lifetime of the solar array. Data sheets were obtained for specific commercial panels. VMPP was evaluated at 45 C (operation at full power, with the cell temperature well above ambient), while VOC was evaluated at -30 C (open circuit at the lowest ambient likely to occur). The results are summarized in Table 1.

The data in Table 1 show that, depending upon the specific technology selected, the dc bus voltage can rise more than 50% higher than the design value for normal full-power operation. This in turn requires that the energy processor connected to the dc bus be conservatively designed for voltage limits in terms of the switching devices selected and transient voltage limiters used.

An additional observation regarding PV cells is that their short-circuit currents are well-defined, and not excessively greater than their MPP currents (IMPP). Table 2 shows data for the currents of the same panels used in Table 1. DC bus conductors will generally be sized for low energy loss at IMPP, so it is likely that ISC will be well within the thermal limits for the bus. These observations lead to the proposed method [8] of achieving a shutdown condition for a solar array in full sunlight by application of a short-circuit using a shunt switch, rather than requiring the dc bus to withstand the open-circuit voltage.

TABLE 1

<table>
<thead>
<tr>
<th>Type of Solar Panel</th>
<th>VMPP at 45 C</th>
<th>VOC at -30 C</th>
<th>VOC / VMPP</th>
</tr>
</thead>
<tbody>
<tr>
<td>c-Si (AstroPower AP-1106)</td>
<td>14.1 V</td>
<td>25.4 V</td>
<td>1.8</td>
</tr>
<tr>
<td>poly-Si (Solerex MSX-5)</td>
<td>15.2 V</td>
<td>25.0 V</td>
<td>1.65</td>
</tr>
<tr>
<td>GaAs (Spectorlab GaAs/Ge Single Junction Solar Cell)</td>
<td>0.862 V</td>
<td>1.12 V</td>
<td>1.3</td>
</tr>
<tr>
<td>a-Si (DuPont Apollo DA100)</td>
<td>69.0 V</td>
<td>116.5 V</td>
<td>1.69</td>
</tr>
<tr>
<td>CdTe (First Solar FS-270)</td>
<td>62.2 V</td>
<td>97.7 V</td>
<td>1.57</td>
</tr>
<tr>
<td>CIS (Worth Solar WS 11007/80)</td>
<td>33.9 V</td>
<td>52.8 V</td>
<td>1.56</td>
</tr>
</tbody>
</table>

TABLE 2

<table>
<thead>
<tr>
<th>Type of Solar Panel</th>
<th>ISC at 45 C</th>
<th>ISC at -30 C</th>
<th>ISC / ISC at 45 C</th>
</tr>
</thead>
<tbody>
<tr>
<td>c-Si (AstroPower AP-1106)</td>
<td>6.60 A</td>
<td>7.51 A</td>
<td>1.14</td>
</tr>
<tr>
<td>poly-Si (Solerex MSX-5)</td>
<td>0.270 A</td>
<td>0.294 A</td>
<td>1.09</td>
</tr>
<tr>
<td>GaAs (Spectorlab GaAs/Ge Single Junction Solar Cell)</td>
<td>28.6 mA</td>
<td>30.9 mA</td>
<td>1.08</td>
</tr>
<tr>
<td>a-Si (DuPont Apollo DA100)</td>
<td>1.34 A</td>
<td>1.69 A</td>
<td>1.26</td>
</tr>
<tr>
<td>CdTe (First Solar FS-270)</td>
<td>1.07 A</td>
<td>1.24 A</td>
<td>1.16</td>
</tr>
<tr>
<td>CIS (Worth Solar WS 11007/80)</td>
<td>2.22 A</td>
<td>2.53 A</td>
<td>1.14</td>
</tr>
</tbody>
</table>
IV. VOLTAGE CLAMPING SWITCH

A. Centralized vs. Distributed Architectures

Possible applications of the proposed voltage clamping switch are shown in Fig. 1. The architecture assumes panel strings of length \( n \), with \( m \) strings paralleled on the dc collection bus and feeding a central inverter (or group of inverters). The inverter(s) supply a total bus capacitance denoted by \( C_0 \). The string diodes \( D_1 \ldots D_m \) and fuses \( F_1 \ldots F_m \) may, or may not, be required by the array design philosophy. However, if the distributed shunt switches \( (S_1 \ldots S_m) \) shown in Fig. 1 are to be used, the string series diodes will need to be added if not already present. These diodes allow the closure of a string shunt switch without blowing the fuse, or otherwise forcing the string-level switch to carry the short-circuit current of the entire array.

An alternative placement of the shunt switch is indicated by \( S_0 \), located at the central inverter(s). This switch, when closed, will carry the entire array short-circuit current, but does not necessarily need an associated series diode. \( S_0 \) will also carry the transient discharge current from the bus capacitance \( C_0 \). It should be cautioned that the most common “voltage-sourced” inverter topologies cannot remain connected to an energized ac grid while \( S_0 \) is activated. The anti-parallel diodes in the internal inverter switching devices demand that the dc-side voltage exceed the peak value of the ac-side voltage; therefore, operation of \( S_0 \) would need to be coordinated with opening of the ac-side contactor. This conflict could also be resolved by introducing a series diode between \( S_0 \) and the inverter(s).

Either the distributed shunt switch structure, or the central shunt switch, may be selected to positively limit the maximum dc bus voltage. It is also possible to implement both approaches shown in Fig. 1 at the same time for the sake of redundancy. Redundancy may also be obtained by paralleling additional switching devices at each location.

The central switch has the advantage that it can be integrated within an inverter, thus sharing its cabinet and control power. However, it should also be noted that the shunt switch will need to remain closed for an indefinite amount of time without the availability of any grid power in the event of grid outage. The distributed shunt switches provide a convenient means of disconnecting individual strings, and by their distributed nature allow easy dissipation of their on-state conduction losses. The distributed switches will require communication from the central control point to the string level, but could be readily integrated with string-level performance monitoring systems.

B. Shunt Switch Design Requirements

1) General Requirements

The general requirements for the shunt switching device are summarized:

1) It must be very reliable, and preferably fail in a short-circuit condition.
2) Only unidirectional voltage block and current conduction is needed.
3) Switching and conduction losses are not relevant, except for design of its heat-removal system.
4) Low off-state leakage current.
5) Low (or zero) on-state gate power requirements.

The silicon devices considered for the shunt switch were the IGBT, the thyristor family, including the MCT, and the power JFET. The IGBT initially appeared attractive, and both
batteries and ultra-capacitors were considered to maintain on-state gate bias during an extended grid outage, but this approach was ultimately rejected as both too expensive and not certain to reliably keep the shunt switch activated throughout an extended grid outage, and over a 20-year lifetime. The MCT and power JFET could maintain an on-state at zero gate voltage, but the required devices were not readily available. The standard thyristor (SCR) was chosen for a prototype implementation, with an IGBT used to provide turnoff of the SCR. A gate-turn-off (GTO) thyristor is an alternative. Fig. 2 shows a power circuit for a shunt switch implementation at the string level.

2): Sizing the Thyristor

In Fig. 2, SCR1 is the shunt switch. It must be sized to support the highest working bus voltage, and when triggered, the string short-circuit current. There is no difficulty in finding thyristors to meet these requirements for arrays operating below 2000 V. The control circuit must contain a sufficient energy store (not shown) to reliably fire the thyristor when rising bus voltage necessitates activation of the shunt switch. This can be implemented by including sufficient bypass capacitance in the control circuit’s low-voltage power supply to provide the energy for a single gate firing pulse strong enough to achieve the thyristor’s full di/dt rating. Any insulation sufficient to produce an string-level I_sc greater than the thyristor holding current will maintain the shunt switch activated indefinitely, without any other source of auxiliary power. The switching speed of the thyristor is not important to this application, so the more rugged “rectifier grade” devices may be used. Sufficient heat removal for sustained operation at I_sc is needed.

3): Control Power

A subtle design requirement is that the control power supply must somehow acquire enough stored energy for a gate firing pulse faster than an open-circuited array can bring the bus voltage up to dangerous levels. The highest dvbus/dt deemed possible may determine the amount and type of power supply needed for the control circuit. The most pessimistic scenario would be for the shunt switches on an array in full sunlight, and with the ac grid disabled, to somehow turn off. With the only obvious source of control power being the array itself, there would be a race between reacquisition of control power and functionality of the control circuit on one hand, and the rate-of-rise of the bus voltage on the other.

The purpose of the controller is activation of the shunt switch when needed, primarily at the moment of ac grid failure and inverter shutdown. Low-voltage control power may be derived from the dc bus with a simple, but inefficient, shunt regulator, or a more complex switching step-down converter. Either way, the standby current drain of the control power supply will also be a design criterion because it impacts the array energy collection efficiency. Additional current drains are indicated in Fig. 2, due to the voltage dividers producing signals “VM1” and “VM2.” These signals are needed by the control circuit to monitor the dc bus voltage and the energy store in C1, and may add significantly to the standby drain of the control circuit.

4): Turnoff of the Shunt Switch

Turnoff capabilities must be provided for SCR1 when normal operation of the array is to be restored. This event would only occur at a time when the ac grid is stabilized at its normal voltage level, so energy for the turnoff of SCR1 is available from this source. The technique illustrated in Fig. 2 involves the following sequence of events: Assuming a restart from a midday shutdown, 1) the dc bus is energized to a portion of its normal level, 2) this provides control power, 3) capacitor C1 is charged to the dc bus voltage, and 4) when the controller determines that C1 is adequately charged, and when it receives an (optional) external command to do so, provides a gating pulse to the IGBT Q1. The pulsed turn-on of Q1 forces a reverse voltage on SCR1 equal to the capacitor voltage v_c. C1 is then discharged by the string short-circuit current until SCR1 is no longer reverse biased. The turnoff time provided to the thyristor is given by

\[ t_{off} = \frac{V_{CO} C_1}{I_{sc}} \]  

(1)

where \( V_{CO} \) is the initial capacitor voltage. This is the design equation for selecting the capacitor value required.

Shunt switch turnoff is anticipated to be an infrequent event, so the charging time for C1, determined by R1, is not critical and might be several seconds. A lengthy charging time minimizes the current which must be supplied to the dc bus for turnoff of the shunt switches. A small auxiliary rectifier, supplied by the grid, could be used to turnoff the shunt switches, or inverter control action could be used to back feed the bus. As mentioned, the turnoff could be triggered by a signal sent to each controller, or it could simply be programmed to occur upon the raising of the bus voltage to the required minimum \( V_{CO} \). Note that this technique imposes a momentary reverse voltage on the panel string; if panel shunt diodes are being used, a GTO thyristor must be used instead. IGBT Q1 is selected with voltage and current ratings determined by the maximum bus voltage and string short-circuit current, but due to its infrequent use, will not need a heat removal system.

5): The Controller

The controller itself should be designed to use a minimal standby current, allowing a simple shunt regulator to give adequate standby power consumption. The controller needs to monitor the dc bus voltage, and respond to an excursion beyond its trip point with a response time in accordance with the highest \( dvbus/dt \) deemed possible. The controller must also monitor the voltage on C1 so switch turnoff is not attempted prematurely, dissipating the charge in C1. Low-cost micro controllers are available to address these requirements quite well. The shunt switch controller is also a good point at which to implement string level monitoring and communications with a central control point.
6): Controller Response Time Requirement

The time requirement for the controller’s response to a rising bus voltage may be estimated as follows. The rate-of-rise of the bus voltage is the array current divided by the bus capacitance (primarily the inverter-supplied $C_0$). A conservative estimate is based on the array short-circuit current.

$$\frac{dv_{BUS}}{dt} = \frac{mI_{SC}}{C_0}$$  \hspace{1cm} (2)

In (2), $C_0$ is the total bus capacitance, and $mI_{SC}$ is the total array current for $m$ strings. The purpose for $C_0$ is bypassing the inverter switching-frequency currents, so it will be sized based on the maximum acceptable ripple voltage on the dc bus. Approximating the ripple current as having an amplitude equal to the normal dc bus current, the peak-peak ripple voltage will be:

$$\Delta v_{BUS,p-p} \approx \frac{mI_{MPP}}{C_0 f_{SW}}$$  \hspace{1cm} (3)

where $f_{SW}$ is the inverter switching frequency. Assume that $C_0$ has been sized according to the criteria of (3), and substitute (3) into (2) for an estimate of the worst-case rate-of-rise of the bus voltage.

$$\frac{dv_{BUS}}{dt} \leq \frac{I_{SC}}{I_{MPP}} \cdot \Delta v_{BUS,p-p} \cdot f_{SW}$$  \hspace{1cm} (4)

As an example application of (4), if 5% ripple voltage is allowed on a 1000-V bus, with an inverter frequency of 4 kHz and an $I_{SC}/I_{MPP}$ ratio of 1.25, $dv_{BUS}/dt$ is 0.25 V/$\mu$s. A controller response time of 100 $\mu$s would allow a bus-voltage overshoot of only 25 V. This suggests there will be no difficulty obtaining a low-power, low-cost micro controller to implement this function.

V. EXPERIMENTAL TESTING OF THE CLAMPING SWITCH

A prototype shunt switch was designed and experimentally tested to verify its suitability for reliably reducing the voltage swing on the dc bus at open circuit. For this purpose, the following values were assumed for a single string in a utility-scale array: $V_{MPP} = 400$ V, $V_{OC} > 600$ V, $I_{MPP} = 10$ A and $I_{SC} = 13$ A. Such a case might arise in a design intended to operate within the voltage limitations of 600-V rated components. The controller trip point was selected to be 500 V, below the system rating with a safety factor, and high enough to avoid nuisance tripping. Fig. 3 shows the experimental configuration. The panel string was simulated by a 600-V power supply in series with a 23-$\Omega$ resistor. The inverter load on the dc bus is simulated with a 46-$\Omega$ resistor; its sudden removal is simulated by opening switch S1. Switch S2 and the auxiliary supply shown are used for re-energizing the dc bus to turn off.
the shunt switch. The voltage dividers used for sensing purposes, shown in Fig. 2, are actually present, but not shown in Fig. 3 for clarity.

The dc bus capacitance was calculated in accordance with (2)-(4). The value shown, 100 μF, would allow an estimated 22 V_{pp} (on a 400-V bus) with a 4.5-kHz inverter.

Fig. 4 shows the clamp turn-on event. At about 2 ms before the screen center, S1 is opened, simulating the abrupt loss of the dc bus load, such as would occur if the inverter were shut down. The bus voltage rises from the normal 400 V, and the shunt switch trips at its programmed value of 500 V. The simulated string current is also shown in Fig. 4. It initially declines as the bus voltage rises, and then jumps to its short-circuit value (26 A) when the shunt clamp is turned on. This current later decays to the power supply current limiter setting of 13 A.

Fig. 5 shows the clamp turnoff event. To initiate turnoff, the dc bus must first be pre charged from an external source, in this case, by closing S2 and using the auxiliary power supply in Fig. 3. A pre charge voltage of 220 V was used. R1-C1 have a 1-sec time constant, so pre charge will take several seconds. When the controller senses that there is adequate charge on C1 to turn off the SCR, and when it receives an external command, it turns on the IGBT for about 160 μs to complete the turnoff of SCR1. Note that a series diode was added to the IGBT so that it has bi-directional blocking capability. This feature is not essential, but it keeps C1 from accumulating a negative charge during normal operation of the panels. The quiescent condition for C1 is near-zero charge during normal operation of the solar array.

The controller used in the experimental clamp is based on the PIC16F684-E/P micro controller operating with a 4-MHz clock frequency. Power for the micro controller and its associated gate drivers is derived directly from the dc bus using a dissipative shunt regulator. The total standby current drain on the dc bus for the power supplies and the metering circuits is 1.8 mA at 400 V. The voltage trip points are readily re-programmable.

VI. CONCLUSIONS

The improving economics of PV panels need to be matched with improvements in the first cost, reliability and energy efficiency of the dc bus components. Careful design of the dc bus with regard to the distribution of its conductor volume and physical positioning of its components will lower ohmic losses and first costs. Further reduction in installed cost and operating losses may be gained by maintaining the working bus voltage as high as possible, without exceeding limits set by component ratings or operating standards.

An experimental system rated for 600 V was considered. It could only operate at 400 V, with no margin of safety, due to its high open-circuit voltage. Adding the proposed voltage clamp easily added a 100-V margin of safety to the system. These results suggest that with the added voltage clamp, the number of panels in a string, and thus V_{MPp}, could be substantially increased. This pays off by improving the inverter utilization and lowering ohmic losses (or lowering copper costs) throughout the dc system.

The proposed voltage clamp system provides a useful increase in margin of safety for the operating voltage of the dc system, or alternatively, allows the operating voltage to be set closer to the system limits for a reduction in ohmic losses. A useful avenue for future investigation is the use of this clamp in a protection system to extinguish arcing in the dc bus. This may prove necessary as utility-scale systems evolve towards higher dc operating voltages.

VII. REFERENCES


VIII. BIOGRAPHIES

Penghao Chen (S’08) was born in Tianjin, China. He received the B.Eng. degree in electrical and electronic engineering from the Tianjin University of Technology, Tianjin, China, in 2007. He is currently working the Master Degree in electrical engineering in University of Toledo, Toledo, US. His current research interests include photovoltaic power system and power electronics.

Roger King (S’1972, M’75, SM’90) received the B.SEE, MSEE and PhD degrees from the University of Toledo, Toledo, OH, in 1972, 1975, and 1983, respectively. Prior to returning to graduate school in 1978, he spent several years designing analog instrumentation. He is presently Professor of electrical engineering and computer science at the University of Toledo. He specializes in power electronics teaching and research. His research interests include high-power factor rectifiers, transient modeling techniques for switching converters, and distributed generation/alternative energy systems. Dr. King is a registered Professional Engineer in the State of Ohio, and is a member of Eta Kappa Nu, Tau Beta Pi and Sigma Xi.