ABSTRACT

Does the world need yet another solar inverter concept? Intermediate size inverters have grown; now there is a MegaWatt in a box, and on the other end of the scale, panel level MicroInverters have hit the market. Manufacturers have developed panel and string level DC to DC converters that couple to a large central inverter, and increased attention has been paid to the critical role of the inverter with respect to the economics of solar generated electricity.

Nextronex Energy Systems LLC, formed in 2008 from an established design-engineering firm, looked at the offerings, talked with installers and specifiers, and concluded that the world would benefit from yet another solar inverter concept, one that we call “Distributed Architecture.”

Distributed Architecture goes beyond the inverter and includes companion components that form a complete wiring and control system for utility scale solar arrays. This approach optimizes the performance and reliability of a solar array, reduces engineering and procurement time, and can save installation cost and time. As our industry matures, the focus is shifting from installed cost (still very important) to expected revenue over the life of the array. Financiers have a critical interest in the revenue stream, uptime, and operation and maintenance cost of solar projects, and we believe that our inverter and wiring technology offers the most cost-effective solution to maximizing the revenue stream of the array.

1. SOLAR INVERTER TECHNICAL APPROACHES

Fig. 1 represents the continuum of solar inverters available in the market place today. The bookends are a panel level microinverter on the left, and a MegaWatt in a box on the right. This follows the array size as you go up from a panel level inverter through iterations of string level inverters, to large central inverters. All things being equal, the larger inverters are more cost effective and more efficient. But there is more to the story than cost and efficiency.

2. MICROINVERTERS

At the microinverter level, the driver is safety and ease of installation. On residential and small commercial systems, microinverters eliminate DC wiring with potentially hazardous voltages. Case studies have identified DC arc flash as a contributor to fires, and worse, fire brigades will not attempt to douse a structure with a PV array on the roof, because even with the meter pulled, there are still hazardous voltages present.

A synchronous microinverter will not export any power, or have any AC voltage at the output if the AC power is not on. Proper education and labeling can insure that fire brigades are able to protect a structure once the meter has been pulled. Another benefit of the microinverter, especially when mounted to the panel, is the ease of installation.

The disadvantages of the microinverter are cost, efficiency, and longevity. Cost will come down, and longevity can only be assessed over time.

3. CENTRAL INVERTERS (MEgAWATT IN A Box)

At the MegaWatt in a box level, efficiency can be quite high, and the high voltage interconnect can be integral to the box. The challenge can be installation cost and
logistics. Basically, every solar panel must be connected to this inverter box, via a network of DC runs, combiners, DC trunk lines, and Recombiners, all of which must be custom engineered and specified by the designers. Depending on the panel type, a megawatt field will consist of 4000 to over 13000 panels, covering from 3 to 8 acres, and the DC wiring can get quite complex and difficult to diagnose, and have significant power losses.

The MegaWatt in a box is a large container. It requires a substantial foundation and large equipment to transport and set it in place. By its nature, it’s a shadow producer, so it must be to the North of the array, or removed some distance from the array.

Some of the newer central inverters incorporate a form of Master/Slave switching, which does improve energy harvesting under marginal conditions, but redundancy and reliability is not necessarily improved, because the box has a number if interdependencies between modules, including cooling, and control.

4. DC-DC UPCONVERTERS (STRING LEVEL) FEEDING A CENTRAL INVERTER

This is a unique approach to allow string level MPPT management, then feeding a constant voltage DC bus to a large central inverter. There is a lot of flexibility in this approach, and string level control is thought to be a desirable attribute. String level monitoring is a desirable attribute, and that is enabled with this system.

The disadvantages are cost, efficiency, and reliability – at least at the central inverter level.

DC to DC conversion involves “chopping”; sampling the incoming DC at a high frequency (typically 100 kHz or more), using a small high frequency transformer to step this voltage up, then filtering the output to return to a ripple-free DC waveform. Additional circuitry is used to manage the MPPT at the panel or string level, then feeding a constant voltage DC (which must be identical for each panel or string) to a combiner as input to a central inverter. In this configuration, the inverter needs no MPPT tracking capability, and the various system voltages can be optimized.

The problem is cost, efficiency, and reliability. The best DC-DC converters are 97 % efficient, and at the panel level, you add another cost component to the system.
Advocates of this approach maintain that you will get more energy from the array by optimizing the MPPT at the panel or string level, because shading, panel mismatch, and uneven panel degradation may affect the ability to centrally manage the MPPT. There are also claims that one can mix and match solar panels in an array. These are not substitutes for proper engineering and layout and quality panels.

5. THE NEXTRONEX DISTRIBUTED ARCHITECTURE

The Nextronex approach is a hybrid. We start with a highly-efficient, robust inverter that is derived from a variable speed AC motor drive, package it in a low profile cabinet that allows placement flexibility, and parallel these on a DC bus to accommodate any array size from 100 kW up through 1.5 MegaWatts (Fig. 2). (Note that larger fields are simply multiples of 1 to 1.5 Megawatts, further enhancing the flexibility and reliability of the design.)

The operational strategy can be summarized very simply: We can funnel the entire array output to as few inverters as needed at any instant in time.

The Nextronex inverter is a transformerless design, that nonetheless is coupled through a transformer for isolation. There is a unique efficiency advantage of this design, because the coupling transformer can be custom wound for the application, and in larger installations, the separate transformer functions (isolation and step-up to distribution voltage) can be combined in one multi-primary unit, eliminating a stage, which adds at least 2 % efficiency to the system. We’ll return to the discussion of operating voltages again later.

Connecting the solar array to the bus is accomplished via multi-input zone boxes that are physically attached to the bus, and allow up to 4 fused inputs. With most panel types, each input will accommodate around 5 kW, so each zone box will contribute about 20 kW of panels. The zone boxes incorporate fuses on both + and – legs (required for ungrounded operation), optional CT’s, an MOV lightning protection network, and a safety disconnect switch. The output of the CT’s are sent to the smart controller, which controls the overall inverter operation, reads the Zone currents, and summarizes the array performance both on the internal HMI screen, and remotely via the built-in Ethernet connection.

Fig. 3 shows the default system screen and Fig. 4 shows a screen of the instantaneous row currents, useful as a diagnostic tool to insure that the array is functioning as designed.

All the components in the Nextronex system are approved for 1000 V DC operation. The National Electrical Code allows this voltage on all installations other than one and two family dwellings, and the UL 1703 panel standard also recognizes this voltage level. Operating at a 1000 V string voltage reduces the number of home runs by 40 %, and reduces IR losses, so this is another key advantage of the Nextronex system.
In the Nextronex system, the entire array’s output is available on a DC Bus or Power Strip. Inverters are connected to this bus, preferably placed symmetrically and evenly along the bus. A master controller (smart controller) controls the operation of the inverters based on the instantaneous power available from the array.

The AC outputs of the inverter are coupled together through isolation transformers, or a multi-primary load center, which accomplishes the same thing and provides step-up to distribution voltages.

6. BUS DESIGN

This section discusses possible design scenarios for assigning “copper” to the dc energy collection system. First cost is assumed proportional to the weight (or volume) of copper conductor used; operating cost is assumed proportional to the total energy lost in the conductor. The solar array is modeled as a two-dimensional distribution of many equal-valued current sources having a small spacing. These assumptions allow considerations of first-cost vs. payback to guide the choices of the total amount of conductor used, the optimum distribution of the conductor used, and the selection of the optimal location of the tap point where the inverter (or boost converter) will be connected to raise the voltage from the array level to a higher utility level. These assumptions are appropriate for a utility-grade solar field in which a very large array of well-matched panels receive uniform insolation. The voltage profile across the field is also predicted and is useful as an additional design parameter.

6.1 Row Conductor Arrangements

Three possible row conductor arrangements are illustrated in Figs. 5, 6 and 7. They are denoted “constant area” (CA) conductors, “proportional area” (PA) conductors and “constant voltage drop” (CVD) conductors. CA conductors are simply bus bars having uniform cross section and extending the length (L) of the row. Distance along the row is measured by the variable “x,” with the tap point denoted by “X.” Assuming a total row current of IRow, the current at any point in the bus is given by:

\[ i(x) = \frac{I_{\text{ROW}}}{L} x \quad \text{for} \quad 0 \leq x < X \]

and

\[ i(x) = \frac{I_{\text{ROW}}}{L} (L - x) \quad \text{for} \quad X < x \leq L \]

PA conductors are proportioned so that the cross section of the bus bar is proportional to \( i(x) \) as given by (1). This structure is approximated in practice by laminating many thin strips of various lengths to form the bus bar, or by using many identical individual wires to connect the panels to the tap point. The PA bus concentrates the available copper in its portions carrying the higher currents. The CVD bus is assumed to be subdivided into many individually insulated sections, each carrying the current from a section of the total row length dx. The CVD bus is approximated in practice by using wire of various gauges, concentrating the available copper on the wires carrying the current from the farthest distances along the row. The CVD bus is designed so that each individual wire has the same resistance and produces the same voltage drop along its total length, and hence will equalize the individual panel voltages, given matched panels.

6.2 CA Bus Analysis

Given a chosen bus cross section of \( A_{cu} \) and length \( L \), the total volume of copper is calculated:

\[ V_{cu} = 2A_{cu}L \]

The resistance per unit length of one bus bar is found in terms of the conductivity of the material (\( \sigma_{cu} \)):

\[ R'(x) = \frac{1}{\sigma_{cu} A_{cu}} = \frac{2L}{\sigma_{cu} V_{cu}} \]

The corresponding power loss in both bus bars for the entire row is:

\[
P_{\text{LOSS}} = 2 \int_{x=0}^{x=X} \left( \frac{I_{\text{ROW}}}{L} x \right)^2 \frac{2L}{\sigma_{cu} V_{cu}} \, dx + 2 \int_{x=X}^{x=L} \left( \frac{I_{\text{ROW}}}{L} (L - x) \right)^2 \frac{2L}{\sigma_{cu} V_{cu}} \, dx
\]

\[
P_{\text{LOSS}} = \frac{4I^2_{\text{ROW}} L^2}{\sigma_{cu} V_{cu}} \left[ \frac{1}{3} - \frac{X}{L} + \left( \frac{X}{L} \right)^2 \right]
\]

Equation (4) shows that the optimum tap point X with regard to power loss is at the center of the row (X=L/2), and if the more convenient end-of-row tap point is used, the power loss will be 4 times that of a central tap point. It can also be seen that either loss or total conductor volume must increase with the square of the row length. The advantage of lowering total row current (by raising the design voltage) can also be seen clearly in (4). Given a center tap point, the
The relationship between conductor volume and power loss is:
\[ P_{\text{loss,opt}}^{\text{opt}} = \frac{I_{\text{ROW}}^2 L^2}{3 \sigma_c V_{Cu}} \]

The bus voltage profile, assuming a center tap point, is calculated:
\[ V(x) = V_{\text{tap}} + \int_0^{\frac{x}{2}} i(x)R(x)dx = V_{\text{tap}} + \frac{I_{\text{ROW}} L^2}{2 \sigma_c V_{Cu}} \left[ -\frac{1}{2} \left( \frac{x}{L} \right)^2 \right] \]
for \( 0 \leq x \leq L = \frac{L}{2} \)

A symmetric voltage profile will occur on the other side of the tap point. Given a fixed row length, the bus design procedure will be to determine the maximum acceptable voltage variation (\( \Delta V \)) from the center to the row end and calculate the needed conductor volume from the following:
\[ V_{Cu} = \frac{I_{\text{ROW}} L^2}{2 \sigma_c \Delta V} \]

6.3 PA Bus Analysis

The current distribution vs. position in the PA bus is given by (1), but the bus cross section is proportioned to the current at each location, as indicated in Fig. 6 for the general case of an off-center tap point. The ratio of the two maximal cross sections at the tap point is therefore:
\[ A_{\text{Cu, max}} = A_{\text{Cu, max}} \frac{i(x^+)}{i(x^-)} = A_{\text{Cu, max}} \frac{L - X}{X} \]

The total volume of conductor in both bus bars is:
\[ V_{Cu} = \frac{1}{2} A_{\text{Cu, max}} \left[ L^2 - 2LX + 2X^2 \right] \left( L - X \right) \]

The resistance per unit length of the bus bar is:
\[ R(x) = \frac{1}{\sigma_c A_{\text{Cu}}(x)} = \frac{1}{\sigma_c A_{\text{Cu, max}}} \frac{L - X}{x} \]
for \( 0 < x < L \)

The total power loss in both bus bars is found in the same manner as in (4):
\[ P_{\text{loss}} = \frac{I_{\text{ROW}}^2 L^2}{4 \sigma_c V_{Cu}} \left[ 1 - \frac{X}{L} + 2 \left( \frac{X}{L} \right)^2 \right] \]

As with the CA bus, the optimum tap point for the PA bus is at the center (\( X = L/2 \)), and the penalty for placing the tap at either end is a 4-times increase in loss or conductor volume. The optimum power loss design for the PA bus results in:
\[ P_{\text{loss,opt}} = \frac{I_{\text{ROW}}^2 L^2}{4 \sigma_c V_{Cu}} \]

The voltage profile for the PA bus with center tap point is calculated in the same manner as in (6):
\[ V(x) = V_{\text{tap}} + \frac{I_{\text{ROW}} L^2}{2 \sigma_c V_{Cu}} \left[ 1 - 2 \left( \frac{x}{L} \right) \right] \]
for \( 0 \leq x \leq X = L/2 \)

Again, the profile for the other side of the center is symmetrical. Examination of (6) and (13) shows that the CA and PA buses have the same center-to-end voltage drop for the same conductor volume, and that the design equation given in (7) is also useful for the PA bus.

6.4 CVD Bus Analysis

By design, the voltage profile along the length of the CVD bus is uniform. This is accomplished by subdividing the bus into many mutually-insulated segments, each having the same end-to-end resistance, and each carrying the same current generated by a small segment of the row panels spanning distance \( dx \). In the following analysis, the location variable \( x \) refers to the small section of panels located at this distance along the row, and to the small portion of bus cross section \( dA_{\text{Cu}} \) which services these panels. The current produced by the panels in \( dx \) (not the total bus current at that point) is:
\[ i(x) = \frac{I_{\text{ROW}}}{L} dx \]
The design of the bus may be approached in terms of its effective one-way resistance $R_{\text{eff}}$, and the acceptable voltage drop $\Delta V$:

$$\Delta V = I_{\text{ROW}} 2R_{\text{eff}}$$

This voltage drop is achieved by assigning a portion ($dA_{Cu}$) of the total available conductor cross section to each region of the row given by:

$$dA_{Cu}(x) = \left( \frac{I_{\text{ROW}}}{L} \right) \left( \frac{2(x - X)}{\sigma_{Cu} \Delta V} \right) \quad \text{for} \quad X < x \leq L$$

Substituting (15) into (16):

$$\frac{dA_{Cu}(x)}{dx} = \left( \frac{|x - X|}{L \sigma_{Cu} R_{\text{eff}}} \right) \quad \text{for} \quad 0 \leq x \leq L$$

The total volume of conductor needed for both bus bars is:

$$V_{Cu} = 2 \int_{x=0}^{L} dA_{Cu}(x) = \int_{x=0}^{L} \frac{2(x - X)}{\sigma_{Cu} \Delta V} dx = \frac{2L^2}{3\sigma_{Cu} R_{\text{eff}}} \left[ 1 - \frac{x}{L} + \frac{X}{L} \left( \frac{X}{L} \right)^2 \right]$$

As with the CA and PA buses, the total volume of conductor minimizes with the tap point at the center ($X=L/2$), and 4 times the minimum conductor volume or minimum $R_{\text{eff}}$ is needed to place the tap at the row end. The resulting minimum conductor volume and total power loss are:

$$V_{Cu,\text{OPT}} = \frac{L^2}{6\sigma_{Cu} R_{\text{eff}}}$$

$$P_{\text{LOSS,OPT}} = 2I^2_{\text{ROW}} R_{\text{eff}} = \frac{L^2}{3\sigma_{Cu} V_{Cu}}$$

The voltage profile is:

$$v(x) = V_{\text{TAP}} + 2I_{\text{ROW}} R_{\text{eff}} = V_{\text{TAP}} + \frac{I_{\text{ROW}} L^2}{2\sigma_{Cu} V_{Cu}}$$

### 6.5 Comparisons Among the Three Bus Designs

Comparisons may be made among the three bus designs on the basis of devoting the same total volume of conductor and using the central tap point in each case. The total power losses are given for the CA by (5), the PA by (12), and the CVD by (20). The CA and CVD consume equal power losses, and the PA consumes $\frac{3}{4}$ of either of these. The CA and PA designs produce identical end-to-center voltage drops, but have different profiles of voltage with respect to position: The CA bus has a quadratic profile (6), while that of the PA bus is linear (13). The CVD by design produces a constant voltage drop and a flat profile. These voltage profiles are illustrated in Fig. 8. The CVD voltage profile (21) shows that it has $1/3$ of the center-to-end voltage drop produced by the CA or PA buses.

Of the designs considered, the PA bus is optimum in terms of total power loss in the bus, although it does not have a flat voltage profile. The CVD bus is optimum in terms of center-to-end voltage drop, and has a flat voltage profile as well. The CA bus is probably the simplest to install. The PA bus could be installed by laminating a number of equally-sized thin conductor strips to approximate the variable cross section bus, or it could be approximated by large numbers of individual wires, all of the same gauge. The CVD bus is difficult to imagine as a laminated bus, but it is approximated by using a number of different individual wires, in a range of gauge sizes, with the largest wires serving the farthest reaches of the row.

### 6.6 Extension to Two Dimensions

A utility scale array will extend significant distances in two directions. Individual rows have thus far been considered, with many individual panel strings paralleled on the row buses. The complete array will have collection buses passing through the array orthogonal to the row buses, with row terminating boxes (the row tap point) connecting the row outputs in parallel at the collection buses. The consideration thus far of three row bus designs can readily be applied to the collection buses as well. From the perspective of usage of bus conductor material, the optimum array layout is a square, with each row terminated in its center at its intersection with the collection bus, also terminated in its center. This final termination point at the center of the square is the ideal location for the power processors which will raise the voltage level from the nominal operating value for the array (perhaps 600-1200 V) to a higher utility distribution level (typically 12-15 kV).

### 6.7 Summary

Three array collection bus designs, shown in Figs. 5, 6 and 7, have been considered from the perspective that their conductor material is a significant first-cost factor in the
design of a utility-sized solar array. These three bus designs have differing difficulties of installation, but each can be reasonably approximated by current installation practices. It has been shown that in all cases, the volume of conductor material needed is proportional to the square of the total current and the square of the linear dimension of the bus. In each case, total power loss and voltage drop are inversely proportional to the conductor volume (Fig. 8). Bus designs have been identified which result in either minimum power loss or flat voltage profile. The penalty for moving the tap point from the center to the end of a collection bus has been quantified.

Fig. 9 shows a practical realization of the central inverter cluster optimized layout. The Nextronex low profile components lend themselves to this layout, which realizes the least amount of copper with the highest collection efficiency.

7. INVERTER SWITCHING ALGORITHM

At the end of a day, before the sun sets and the bus voltage collapses, but still close enough to sunset that only one inverter is running, the controller logs inverter run time and status parameters. The inverter with the least amount of run time is selected to start the next day. The selected lead inverter will start in “Internal MPPT” mode. The other inverters are set to “external MPPT” mode for that day by the controller.

When the sun rises and DC voltage begins building on the bus, the selected inverter wakes up at a pre-determined DC wake up voltage (actually determined in-situ when the system is commissioned). As the voltage rises, and approaches the calculated MPPT value for this array (remember that we’re in open circuit mode at this point, so this voltage will quickly go towards the Voc point), the lead inverter starts to draw current and manages the MPPT for the array. The maximum allowable current for each inverter is 240 amps DC; if (when) the output current equals or exceeds 180 amps for five seconds, a second inverter is brought on-line and told to export 10% of its maximum capability. Following the same timing, this inverter is incremented in 10% intervals. When the 2nd inverter approaches it’s maximum, a third is brought online and increased in the same fashion in 10% increments. This approach was chosen to maintain sufficient headroom for the lead inverter; the one managing the MPPT for the array.

After solar noon, or during any cloud transients, the system will shed inverters based on the lead inverter pulling less than 92 amps for more than two seconds. The second
inverter is decremented in 20% intervals, and if this goes to zero, the third is decremented, and so on.

If an inverter faults, the system recovers by taking that inverter out of the queue (and if it happened to be the lead for that day, the operating parameters of one of the remaining ones is set to MPPT and it takes the lead position). The system can accomplish this quickly enough to avoid bus collapse.

The actual communication and response time of the system is less than 10 milliseconds, and we have never observed a condition where the bus voltage collapsed because of the system response time.

Actual inverter switching is software driven, and utilizes the AC Contactor to bring inverters on or off line. In all cases, the current is rapidly ramped down to zero just prior to contactor opening or closing. This insures a long contactor life, and avoids any line transients.

We show two performance graphs from our 399 kW, three inverter beta installation at the 180th OANG site adjacent to the Toledo Express Airport. These plots are for two days in October 2010, one representing a clear day (Fig. 10), and one representing a cloudy day (Fig. 11). The blue line is the composite array power output, and the red line is the solar intensity (irradiance).

Inspection of these two graphs indicate the seamless transition from one, two, then three inverters, and the excellent MPPT tracking under partly cloudy conditions. This is critical, as the multiple inverter system must respond fast enough to avoid having the DC bus collapse when the sun dips behind clouds.

8. PERFORMANCE

The advantages of the Nextronex Distributed Architecture are due to:

1. Overall system efficiency of 96% or greater including coupling transformer(s)
2. Enhanced uptime and reliability due to distributed architecture
3. Low Light Level advantage by funneling energy to as few inverters as needed
4. Advanced diagnostics and telemetry to insure that the array is in top shape
5. Easy to service inverter, the electronic core can be replaced in 30 minutes

The data that we have collected show an overall system efficiency (DC nameplate rating to actual AC power generated) of 83%, against a PVWatts default value of 77% (0.77).

With the limited data collection to date, we use a combination of actual measurements and calculated data to predict an annual energy collection of 1270 kWh per installed kW, for the climate in Toledo Ohio. This is a significant improvement over the earlier phases on this project.

9. FUTURE WORK

Enhancements to the Nextronex system will be in the form of cost optimization; for example, to insure that the DC bus parameters are matched to the array size, and continual monitoring to validate the energy advantage claims. The smart controller data gathering and telemetry will be refined, and capability of interacting with the smart grid will be implemented as available.

Product enhancements will include the concept of a “voltage clamp” that can help raise the operating voltage of the array while still adhering to the Voc limits (either 600 V or 1000 V), and different inverter sizes to better serve the market.

Finally, advances in semiconductors and capacitors, and other components that enhance reliability, will be evaluated to insure that the inverter and system continue to be state-of-the-art.